CLAIMS

WHAT IS CLAIMED IS:

1. A microcontroller comprising:

a mode terminal for receiving a mode signal to distinguish a normal operation mode and a rewrite operation mode;

an internal nonvolatile memory storing therein a program to be executed during said rewrite operation mode;

a CPU core for generating address signals sequentially, for activating a first chip select signal when the address signals designate a first area, for receiving, during said rewrite operation mode, rewrite data according to the program stored in said internal nonvolatile memory, and for writing the received rewrite data to an electrically rewritable external nonvolatile memory connected to the microcontroller; and

a first selector circuit for receiving the mode signal at a select terminal thereof, for transmitting the first chip select signal to said external nonvolatile memory when the mode signal indicates said normal operation mode, and for transmitting the first chip select signal to said internal nonvolatile memory when the mode signal indicates said rewrite operation mode.

2. The microcontroller according to claim 1, further comprising

an internal volatile memory being accessed by said CPU core, and wherein:

said internal nonvolatile memory storing in advance therein a transfer program for transferring to said internal volatile memory the rewrite data to be written to said external nonvolatile memory and a rewrite program for writing the rewrite data to said external nonvolatile memory; and

during said rewrite operation mode, said CPU core transfer the rewrite data to said internal volatile memory by executing said transfer program, and write the transferred

rewrite data to said external nonvolatile memory by executing said rewrite program.

3. The microcontroller according to claim 1, further comprising

an internal volatile memory being accessed by said CPU core, and wherein:

said internal nonvolatile memory storing in advance therein a transfer program for transferring to said internal volatile memory the rewrite data to be written to said external nonvolatile memory and a rewrite program for writing the rewrite data to said external nonvolatile memory; and

said CPU core transfers the rewrite data and said rewrite program to said internal volatile memory by executing said transfer program, and writes the rewrite data transferred to said internal volatile memory to said external nonvolatile memory by executing the rewrite program transferred to said internal volatile memory.

4. The microcontroller according to claim 1, further comprising

a selector control circuit for disabling the mode signal input via said mode terminal and forcibly outputting to the select terminal of said first selector circuit a level indicating said normal operation mode, when receiving a mode switch signal, wherein

said CPU core outputs the mode switch signal upon completing writing of the rewrite data to said external nonvolatile memory.

5. The microcontroller according to claim 1, further comprising

a second selector circuit for receiving the mode signal at a select terminal thereof, for transmitting a second chip select signal to an external volatile memory connected to the microcontroller when the mode signal indicates said normal operation mode, and for transmitting the second chip select signal to said external nonvolatile memory when the mode signal indicates said rewrite operation mode, wherein

said CPU core activates the second chip select signal when the address signals designate a second area.

6. The microcontroller according to claim 5, further comprising

a selector control circuit for disabling the mode signal input via said mode terminal and forcibly outputting to the select terminals of said first and second selector circuits a level indicating said normal operation mode, when receiving a mode switch signal, wherein

said CPU core outputs the mode switch signal upon completing writing of the rewrite data to said external nonvolatile memory.

7. The microcontroller according to claim 1, further comprising

an interface circuit for receiving the rewrite data to be written to said external nonvolatile memory via an external terminal, and wherein

said CPU core controls said interface circuit according to said program to receive the rewrite data.

8. The microcontroller according to claim 7, further comprising

an internal volatile memory being accessed by said CPU core, and wherein

said CPU core transfers the rewrite data to said internal volatile memory via said interface circuit during said rewrite operation mode.

9. The microcontroller according to claim 1, wherein

said CPU core generates an address signal which designates a first area initially after power-on.